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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,508	07/29/2003	Jordan Plofsky	ALTRP082	6910

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EXAMINER	
IQBAL, NADEEM	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,508	PLOFSKY, JORDAN	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Sep-Oct, 03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Theron et al., (U.S. Patent number 6631520).

3. As per claim 1, Theron teaches (col. 3, lines 7-10) an FPGA interface device includes a microcontroller, an on-board FPGA, and a memory. He thus teaches limitations pertain to a PLD device comprising a port for external communication, a microprocessor in communication with the PLD, and a memory being in communication with the microprocessor. He also teaches (col. 3, lines 12-15) the microcontroller executes instructions received from a host system using firmware code loaded into the first memory. He thus teaches limitations pertain to memory that includes a test routine and that the test logic is tested using the test routine under control of the microprocessor.

4. As per claim 2, With reference to a port is a parallel port, a serial port, a USB port or a JTAG port. Theron teaches at (col. 4, lines 25-28).

5. As per claim 3, With reference to memory is part of the programmable logic. Theron teaches at (col. 3, lines 9-11, Fig. 3).

6. As per claim 4, With reference to the memory being part of the microprocessor. Theron teaches at (col. 3, lines 9-11).

7. As per claims 5 & 6, With reference to the microprocessor includes an analysis routine. Theron teaches at (col. 3, lines 13-15).

8. As per claim 7, Theron substantially teaches the limitations as claimed in claim 1 above. He also teaches (col. 3, lines 7-10) an FPGA interface device includes a microcontroller, an on-board FPGA, and a memory. He thus teaches limitations pertain to a PLD device comprising a port for external communication, a microprocessor in communication with the PLD, and a memory being in communication with the microprocessor. He also teaches (col. 3, lines 12-15) the microcontroller executes instructions received from a host system using firmware code loaded into the first memory. He thus teaches limitations pertain to memory that includes a test routine and that the test logic is tested using the test routine under control of the microprocessor.

9. As per claim 8, With reference to a port is a parallel port, a serial port, a USB port or a JTAG port. Theron teaches at (col. 4, lines 25-28).

10. As per claims 9 & 10, With reference to memory is part of the programmable logic. Theron teaches at (col. 3, lines 9-11, Fig. 3).

11. As per claims 11 & 12, With reference to the microprocessor includes an analysis routine. Theron teaches at (col. 3, lines 13-15).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 13-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Theron et al., (U.S. Patent number 6631520) in view of Jacobson (U.S. Patent number 7020598).

14. As per claim 13, Theron teaches (col. 3, lines 7-10) an FPGA interface device includes a microcontroller, an on-board FPGA, and a memory. He thus teaches limitations pertain to a PLD device, an embedded microprocessor and associated memory. He also teaches (col. 3, lines 12-15) the microcontroller executes instructions received from a host system using firmware code loaded into the first memory. He thus teaches limitations pertain to down loading to the memory a test routine. He also teaches (col. 3, lines 12-15) the microcontroller executes instructions received from a host system using firmware code loaded into the first memory. He thus teaches to execute the test routine under control of the microprocessor to test the PLD. Theron does not explicitly disclose sending results from the microprocessor to a test system external to the PLD. Jacobson teaches (col. 3, lines 52-55) diagnostic tests on the PLD and results from the test are collected and transmitted back to the repair center. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the invention of Jacobson into the invention of Theron to be able to send the results from the microprocessor to a test system. This is because Theron clearly teaches an external host system in communication with the microcomputer that performs tests on the PLD and Jacobson teaches collecting the test results and transmitting to a repair center, therefore provides motivation for the stated inclusion.

15. As per claim 14, Theron teaches (col. 3, lines 12-15) the microcontroller executes instructions received from a host system using firmware code loaded into the first memory.

16. As per claim 15, With reference to the results are the raw data. Jacobson teaches (col. 3, lines 52-55) diagnostic tests on the PLD and results from the test are collected and transmitted back to the repair center.

17. As per claims 16 & 17, With reference to downloading to the microprocessor an analysis routine for analyzing the data and executing the analysis routine to produce results. Theron teaches (col. 3, lines 12-15) the microcontroller executes instructions received from a host system using firmware code loaded into the first memory. Jacobson teaches (col. 3, lines 52-55) diagnostic tests on the PLD and results from the test are collected and transmitted back to the repair center.

18. As per claim 18, With reference to memory is part of the programmable logic. Theron teaches at (col. 3, lines 9-11, Fig. 3).

19. As per claim 19, With reference to associated memory is part of the microprocessor. Theron teaches at (col. 3, lines 13-15).

20. As per claim 20, Theron teaches (col. 3, lines 7-10) an FPGA interface device includes a microcontroller, an on-board FPGA, and a memory. He thus teaches limitations pertain to a PLD device, an embedded microprocessor and associated memory. He also teaches (col. 3, lines 12-15) the microcontroller executes instructions received from a host system using firmware code loaded into the first memory. He thus teaches limitations pertain to down loading to the memory a debugging routine. He also teaches (col. 3, lines 12-15) the microcontroller executes instructions received from a host system using firmware code loaded into the first memory. He thus teaches to execute the test routine under control of the microprocessor to test the PLD. Theron does not explicitly disclose sending results from the microprocessor to a host computer

external to the PLD. Jacobson teaches (col. 3, lines 52-55) diagnostic tests on the PLD and results from the test are collected and transmitted back to the repair center. It would have been obvious to a person of ordinary skill in the art to include the invention of Jacobson into the invention of Theron to be able to send the results from the microprocessor to a test system. This is because Theron clearly teaches an external host system in communication with the microcomputer that performs tests on the PLD and Jacobson teaches collecting the test results and transmitting to a repair center, therefore provides motivation for the stated inclusion.

21. As per claim 21, Theron teaches (col. 3, lines 12-15) the microcontroller executes instructions received from a host system using firmware code loaded into the first memory.

22. As per claim 22, With reference to the results are the raw data. Jacobson teaches (col. 3, lines 52-55) diagnostic tests on the PLD and results from the test are collected and transmitted back to the repair center.

23. As per claims 23 & 24, With reference to downloading to the microprocessor an analysis routine for analyzing the data and executing the analysis routine to produce results. Theron teaches (col. 3, lines 12-15) the microcontroller executes instructions received from a host system using firmware code loaded into the first memory. Jacobson teaches (col. 3, lines 52-55) diagnostic tests on the PLD and results from the test are collected and transmitted back to the repair center.

24. As per claim 25, With reference to memory is part of the programmable logic. Theron teaches at (col. 3, lines 9-11, Fig. 3).

25. As per claim 26, With reference to associated memory is part of the microprocessor. Theron teaches at (col. 3, lines 13-15).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)-272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI